HVMOS Device SPICE Modeling Service Questionnaire

Please fill out the following questionnaire. The data you provide in this form is necessary for Simucad to supply you with high quality SPICE models. If you have any questions please contact:

SPICE Modeling Group
Phone 408-654-4337
Fax: 408-330-9293
email: spicemodeling@simucad.com

Contact Person in Your Company

(for technical questions)

NAME: ______________________________

PHONE: ______________________________

FAX: ______________________________

email: ______________________________

Package Part or Wafer Information:

For packaged parts please specify package type:

____

For wafer, please specify:

How many wafers will be supplied?: ______________

Wafer #: ______________________________

Lot#: ______________________________

Are the devices in a scribeline or in a drop-in test die?: __________

____

Please indicate the gate material of the HVMOS devices:

____

Please indicate the dielectric permitivity of the gate insulator (e.g. oxide=3.9): ______________________

Is there a substrate contact?______________

Model Type

Please specify the SPICE model type (For example: Level 3, BSIM3V3, HVMOS, Macro Model etc.)

____

Please specify the circuit simulator(including the version number) for which the models are generated.

____

____

Bias Conditions

Please specify the maximum bias conditions to apply for MODELING purposes. (Make sure the specified bias conditions are not destructive for the shortest channel length device over the temperature.

	NMOS	PMOS
Max VDS:		
Max VGS:		
Max VBS:		
Max IDS:		

Please include measured data plots of IDS/VDSmax @ VBS=0V, IDS/VDSmax @ VBSmax and IDS/VGS @ VBS steps from 0V to VBSmax.

Breakdown Voltages

BVDS (drain to source): ______________________

BVDB: (drain to bulk): ______________________

BVG: (gate): ______________________

Process and Layout Related Information

Please provide the following information for the supplied wafer or the packaged parts.

	NMOS	PMOS
TOX:		
VTO: (indicate measurement conditions)		
NCH: (surface concentration)		
NSUB: (bulk (below surface) concentration)		
XJH: (heavily doped region junction depth)		
XJL: (lightly doped region junction depth)		
HDIF: (middle of contact to n+/p+ mask edge)		
LDIF: (length of lightly doped region)		
RSH: (heavily doped region)		
RD: (lightly doped region)		
RON: (on resistance)		

Temperature Conditions

Please specify the temperature points for devices to be characterized?

(For example: 0 C, 27 C, 85 C): ______________________________

____

Test Chip Information

Please list the HVMOS devices in the test chip. (If there are more than 5 devices please specify only 5 critical devices.):

	NMOS (μm)		PMOS (μm)	
	W	L	W	L
1)				
2)				
3)				
4)				
5)				

(w should include all gate fingers or cylindrical symetry)

Are there area and periphery diode structures to measure Area (CJ) and Sidewall (CJSW) capacitance? (If yes, please indicate the location of these structures on the test chip.)

____

____

Are there structures to measure overlap capacitances?

(If yes, please indicate the location of these structures on the test chip.)

____

____

Is there a Ring Oscillator circuit available for AC model validation? (If yes, please indicate the location of these structures on the test chip.) ______________________________

____

____

Worst Case Corner Information

Please provide the following information for the worst case corner model generation: If the exact numbers are not available please enter the variation in percentage. If data is not available enter: N/A.

	NMOS			PMOS		
	min.	typ.	max	min.	typ.	max
TOX						
VTO						
DL (total diffusion)						
DW (total diffusion)						
RSH (N+ for NMOS) (P+ for PMOS)						
IDSAT (specify IDSAT measured bias conditions and device geometry)						

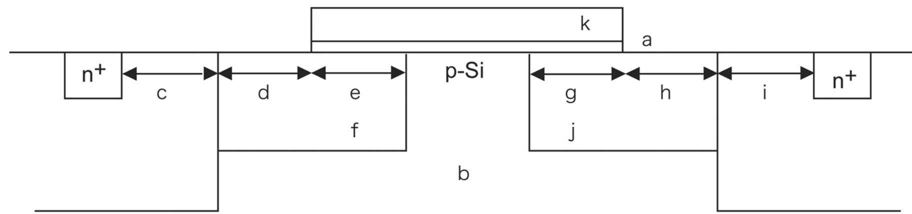
Bias Conditions:

W/L:

	NMOS	PMOS
CJ		
CJSW		
CGDO		
CGSO		

Please add more parameters' variation (such as NCH (surface conc.), NSUB (bulk conc.), UO (mobility), etc.) if available.

For modeling **SYMMETRICAL** structure (HVMOS) devices using HiSIM HV model , the following parameters need to be specified by customers.



Process parameters:

a: TOX (Gate oxide thickness): ______________________

b: NSUBC (Substrate impurity concentration): ____________

c: LDRIFT2 (Length of heavily doped drift region in the source side): ______________________

d: LDRIFT1 (Length of lightly-doped drift region in the source side): ______________________

e: LOVERLD (Gate-source overlap length): ______________

f: NOVER (Impurity concentration in the source overlap region): ______________________

g: LOVERLD (Gate-drain overlap length): ______________

h: LDRIFT1 (Length of lightly-doped drift region in the drain side): ______________________

i: LDRIFT2 (Length of heavily doped drift region in the drain side): ______________________

j: NOVER (Impurity concentration in the drain overlap region) : ______________________

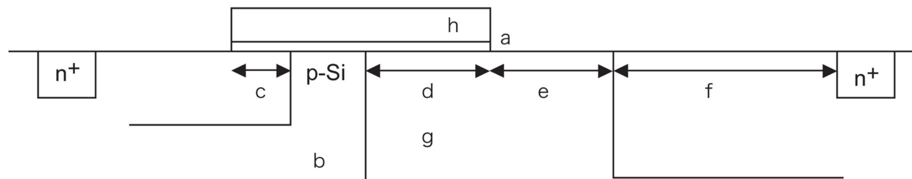
k: RSHG (Gate sheet resistance) : ______________________

Geometrical parameters:

L (Gate length) : ______________________

W (Gate width) : ______________________

For modeling **ASYMMETRICAL** structure (LDMOS) devices using HiSIM HV model , the following parameters need to be specified by customers.



Process parameters:

a: TOX (Gate oxide thickness): ______________________

b: NSUBC (Substrate impurity concentration): ____________

c: LOVER (Gate-source overlap length): ______________

d: LOVERLD (Gate-drain overlap length):______________

e: LDRIFT1 (Length of lightly-doped drift region):__________

f: LDRIFT2 (Length of heavily doped drift region):__________

g: NOVER (Impurity concentration in the overlap region): ______________________

h: RSHG (Gate sheet resistance) = ______________________

Geometrical parameters:

L (Gate length) : ______________________

W (Gate width) : ______________________

HEADQUARTERS

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