

LDMOS Device SPICE Modeling Service Questionnaire

Please fill out the following questionnaire. The data you provide in this form is necessary for Simucad to supply you with high quality SPICE models. If you have any questions please contact:

SPICE Modeling Group
Phone 408-654-4337
Fax: 408-330-9293
email: spicemodeling@simucad.com

Contact Person in Your Company

(for technical questions)

NAME: _____

PHONE: _____

FAX: _____

email: _____

Package Part or Wafer Information:

For packaged parts please specify package type:

For wafer, please specify:

How many wafers will be supplied?: _____

Wafer #: _____

Lot#: _____

Are the devices in a scribeline or in a drop-in test die?: _____

Please indicate the gate material of the LDMOS devices:

Please indicate the dielectric permittivity of the gate insulator
(e.g. oxide=3.9): _____

Model Type

Please specify the SPICE model type (For example: Level 3, BSIM3V3, HVMOS, Macro Model etc.)

Please specify the circuit simulator(including the version number) for which the models are generated.

Bias Conditions

Please specify the maximum bias conditions to apply for MODELING purposes. (Make sure the specified bias conditions are not destructive for the shortest channel length device over the temperature.

NMOS **PMOS**

Max VDS: _____

Max VGS: _____

Max VBS: _____

Please include measured data plots of IDS/VDSmax @ VBS=0V, IDS/VDSmax @ VBSmax and IDS/VGS @ VBS steps from 0V to VBSmax.

Breakdown Voltages

BVDS (drain to source): _____

BVDB: (drain to bulk): _____

BVG: (gate): _____

Process and Layout Related Information

Please provide the following information for the supplied wafer or the packaged parts.

NMOS **PMOS**

TOX: _____

VTO: _____
(indicate measurement conditions)

NCH: _____
(surface concentration)

NSUB: _____
(bulk (below surface) concentration)

XJH: _____
(heavily doped region junction depth)

XJL: _____
(lightly doped region junction depth)

HDIF: _____
(middle of contact to n-/p+ mask edge)

LDIF: _____
(length of lightly doped region)

RSH: _____
(heavily doped region)

RS: _____
(lightly doped region)

RD: _____
(lightly doped region)

Temperature Conditions

Please specify the temperature points for devices to be characterized?

(For example: 0 C, 27 C, 85 C): _____

Test Chip Information

Please list the LDMOS devices in the test chip. (If there are more than 5 devices please specify only 5 critical devices.):

NMOS (μm)		PMOS (μm)	
W	L	W	L

- 1) _____
- 2) _____
- 3) _____
- 4) _____
- 5) _____

Are there area and periphery diode structures to measure Area (CJ) and Sidewall (CJSW) capacitance? (If yes, please indicate the location of these structures on the test chip.)

Are there structures to measure overlap capacitances? (If yes, please indicate the location of these structures on the test chip.)

Is there a Ring Oscillator circuit available for AC model validation? (If yes, please indicate the location of these structures on the test chip.) _____

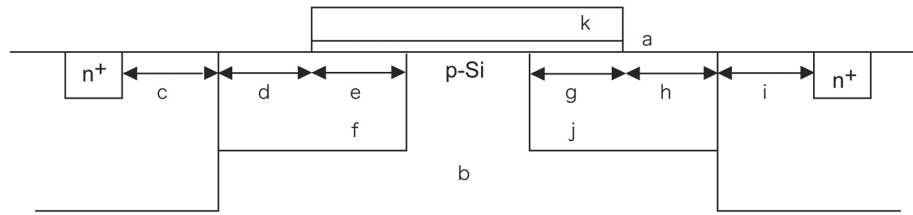
Worst Case Corner Information

Please provide the following information for the worst case corner model generation: If the exact numbers are not available please enter the variation in percentage. If data is not available enter: N/A.

	NMOS			PMOS		
	min.	typ.	max	min.	typ.	max
TOX	_____	_____	_____	_____	_____	_____
VTO	_____	_____	_____	_____	_____	_____
DL	_____	_____	_____	_____	_____	_____
(total diffusion)						
DW	_____	_____	_____	_____	_____	_____
(total diffusion)						
RSH	_____	_____	_____	_____	_____	_____
(N+ for NMOS)						
(P+ for PMOS)						
IDSAT	_____	_____	_____	_____	_____	_____
(specify IDSAT measured bias conditions and device geometry)						
Bias Conditions:						
W/L:						
CJ	_____	_____	_____	_____	_____	_____
CJSW	_____	_____	_____	_____	_____	_____
CGDO	_____	_____	_____	_____	_____	_____
CGSO	_____	_____	_____	_____	_____	_____

Please add more parameters' variation (such as NCH (surface conc.), NSUB (bulk conc.), UO (mobility), etc.) if available.

For modeling **SYMMETRICAL** structure (HVMOS) devices using HiSIM HV model , the following parameters need to be specified by customers.



Process parameters:

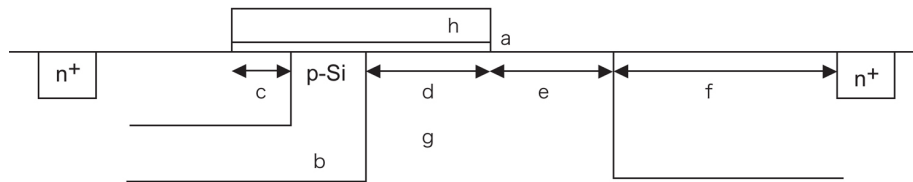
- a: TOX (Gate oxide thickness): _____
- b: NSUBC (Substrate impurity concentration): _____
- c: LDRIFT2 (Length of heavily doped drift region in the source side): _____
- d: LDRIFT1 (Length of lightly-doped drift region in the source side): _____
- e: LOVERLD (Gate-source overlap length): _____
- f: NOVER (Impurity concentration in the source overlap region): _____

- g: LOVERLD (Gate-drain overlap length): _____
- h: LDRIFT1 (Length of lightly-doped drift region in the drain side): _____
- i: LDRIFT2 (Length of heavily doped drift region in the drain side): _____
- j: NOVER (Impurity concentration in the drain overlap region) : _____
- k: RSHG (Gate sheet resistance) : _____

Geometrical parameters:

- L (Gate length) : _____
- W (Gate width) : _____

For modeling **ASYMMETRICAL** structure (LDMOS) devices using HiSIM HV model , the following parameters need to be specified by customers.



Process parameters:

- a: TOX (Gate oxide thickness): _____
- b: NSUBC (Substrate impurity concentration): _____
- c: LOVER (Gate-source overlap length): _____
- d: LOVERLD (Gate-drain overlap length): _____
- e: LDRIFT1 (Length of lightly-doped drift region): _____
- f: LDRIFT2 (Length of heavily doped drift region): _____

- g: NOVER (Impurity concentration in the overlap region): _____
- h: RSHG (Gate sheet resistance) = _____

Geometrical parameters:

- L (Gate length) : _____
- W (Gate width) : _____



HEADQUARTERS

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