

# MOS Device SPICE Modeling Service Questionnaire

Please fill out the following questionnaire. The data you provide in this form is necessary for Simucad to supply you with high quality SPICE models. If you have any questions please contact:

SPICE Modeling Group  
Phone 408-654-4337  
Fax: 408-330-9293  
email: spicemodeling@simucad.com

## Contact Person in Your Company

(for technical questions)

NAME: \_\_\_\_\_

PHONE: \_\_\_\_\_

FAX: \_\_\_\_\_

email: \_\_\_\_\_

## Package Part or Wafer Information:

For packaged parts please specify package type:

\_\_\_\_\_  
\_\_\_\_\_

For wafer, please specify:

How many wafers will be supplied?: \_\_\_\_\_

Wafer #: \_\_\_\_\_

Lot#: \_\_\_\_\_

Are the devices in a scribeline or in a drop-in test die?: \_\_\_\_\_

\_\_\_\_\_

## Model Type

Please specify the SPICE model type (For example: BSIM1, BSIM2, BSIM3V3, etc.) \_\_\_\_\_

\_\_\_\_\_

Please specify the circuit simulator(including the version number) for which the models are generated.

\_\_\_\_\_

\_\_\_\_\_

## Bias Conditions

Please specify the maximum bias conditions to apply for MODELING purposes. (Make sure the specified bias conditions are not destructive for the shortest channel length device over the temperature.

NMOS                  PMOS

Max VDS: \_\_\_\_\_

Max VGS: \_\_\_\_\_

Max VBS: \_\_\_\_\_

Please include measured data plots of  $I_{DS}/V_{DSmax}$  @  $V_{BS}=0V$ ,  $I_{DS}/V_{DSmax}$  @  $V_{BSmax}$  and  $I_{DS}/V_{GS}$  @  $V_{BS}$  steps from  $0V$  to  $V_{BSmax}$ .

## Temperature Conditions

Please specify the temperature points for devices to be characterized?

(For example: 0 C, 27 C, 85 C): \_\_\_\_\_

\_\_\_\_\_

## Process and Layout Related Information

Please provide the following information for the supplied wafer or the packaged parts.

NMOS                  PMOS

TOX: \_\_\_\_\_

VTO: \_\_\_\_\_

NCH: \_\_\_\_\_  
(surface concentration)

NSUB: \_\_\_\_\_  
(bulk (below surface) concentration)

XJ: \_\_\_\_\_  
(junction depth)

HDIF: \_\_\_\_\_  
(middle of contact to gate (poly) distance)

RSH: \_\_\_\_\_

## Test Chip Information

Please list the MOS devices in the test chip. (If there are more than 10 devices please specify only 10 critical devices.):

	NMOS ( $\mu\text{m}$ )		PMOS ( $\mu\text{m}$ )	
	W	L	W	L
1)	_____	_____	_____	_____
2)	_____	_____	_____	_____
3)	_____	_____	_____	_____
4)	_____	_____	_____	_____
5)	_____	_____	_____	_____
6)	_____	_____	_____	_____
7)	_____	_____	_____	_____
8)	_____	_____	_____	_____
9)	_____	_____	_____	_____
10)	_____	_____	_____	_____

Are there area and periphery diode structures to measure Area (CJ) and Sidewall (CJSW) capacitance? (If yes, please indicate the location of these structures on the test chip.)

\_\_\_\_\_

\_\_\_\_\_

Are there structures to measure overlap capacitances? (If yes, please indicate the location of these structures on the test chip.)

\_\_\_\_\_

\_\_\_\_\_

Is there a Ring Oscillator circuit available for AC model validation? (If yes, please indicate the location of these structures on the test chip.) \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

## Worst Case Corner Information

Please provide the following information for the worst case corner model generation: If the exact numbers are not available please enter the variation in percentage. If data is not available enter: N/A.

	NMOS			PMOS		
	min.	typ.	max	min.	typ.	max
TOX _____	_____	_____	_____	_____	_____	_____
VTO _____	_____	_____	_____	_____	_____	_____
DL _____ (total diffusion)	_____	_____	_____	_____	_____	_____
DW _____ (total diffusion)	_____	_____	_____	_____	_____	_____
RSH _____ N+ for NMOS) P+ for PMOS)	_____	_____	_____	_____	_____	_____
IDSAT _____ (specify IDSAT measured bias conditions and device geometry)	_____	_____	_____	_____	_____	_____

### Bias Conditions:

W/L: \_\_\_\_\_

CJ \_\_\_\_\_

CJSW \_\_\_\_\_

CGDO \_\_\_\_\_

CGSO \_\_\_\_\_

Please add more parameters' variation (such as NCH (surface conc.), NSUB (bulk conc.), UO (mobility), etc.) if available.



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