

SOI Device SPICE Modeling Service Questionnaire

Please fill out the following questionnaire. The data you provide in this form is necessary for Simucad to supply you with high quality SPICE models. If you have any questions please contact:

SPICE Modeling Group
Phone 408-654-4337
Fax: 408-330-9293
email: spicemodeling@simucad.com

Contact Person in Your Company

(for technical questions)

NAME: _____

PHONE: _____

FAX: _____

email: _____

Package Part or Wafer Information:

For packaged parts please specify package type:

For wafer, please specify:

How many wafers will be supplied?: _____

Wafer #: _____

Lot#: _____

Are the devices in a scribeline or in a drop-in test die?: _____

Model Type

Please specify the SPICE model type (For example: BSIM3SOI, etc.) _____

Please specify the circuit simulator(including the version number) for which the models are generated.

Bias Conditions

Please specify the maximum bias conditions to apply for MODELING purposes. (Make sure the specified bias conditions are not destructive for the shortest channel length device over the temperature.

NTYPE PTYPE

Max VDS: _____

Max VGS: _____

Max VBS: _____

Max VBG: _____

Please include measured data plots of IDS/VDSmax @ VBG=0V, IDS/VDSmax @ VBGmax and IDS/VGS @ VBG steps from 0V to VBGmax.

Temperature Conditions

Please specify the temperature points for devices to be characterized?

(For example: 0 C, 27 C, 85 C): _____

Process and Layout Related Information

Please provide the following information for the supplied wafer or the packaged parts.

NTYPE PTYPE

TOX: _____

TOXBG: _____

VTO: _____

NCH: _____
(surface concentration)

NSUB: _____
(bulk (below surface) concentration)

XJ: _____
(junction depth)

HDIF: _____
(middle of contact to gate (poly) distance)

RSH: _____

Test Chip Information

Please list the SOI devices in the test chip. (If there are more than 10 devices please specify only 10 critical devices.):

	NTYPE (μm)		PTYPE (μm)	
	W	L	W	L
1) _____				
2) _____				
3) _____				
4) _____				
5) _____				
6) _____				
7) _____				
8) _____				
9) _____				
10) _____				

Are there area and periphery diode structures to Sidewall (CJSW) capacitance? (If yes, please indicate the location of these structures on the test chip.) _____

Are these devices fully or partially depleted SOI devices? _____

Are there structures to measure overlap capacitances? (If yes, please indicate the location of these structures on the test chip.) _____

Is there a Ring Oscillator circuit available for AC model validation? (If yes, please indicate the location of these structures on the test chip.) _____

Worst Case Corner Information

Please provide the following information for the worst case corner model generation: If the exact numbers are not available please enter the variation in percentage. If data is not available enter: N/A.

	NTYPE			PTYPE		
	min.	typ.	max	min.	typ.	max
TOX _____						
TOXBG _____						
VTO _____						
DL _____ (total diffusion)						
DW _____ (total diffusion)						
RSH _____ (N+ for NTYPE) (P+ for PTYPE)						
IDSAT _____ (specify IDSAT measured bias conditions and device geometry)						
Bias Conditions:						
W/L:						
CJ _____						
CJSW _____						
CGDO _____						
CGSO _____						

Please add more parameters' variation (such as NCH (surface conc.), NSUB (bulk conc.), UO (mobility), etc.) if available.



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